Layer Zero Detector

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DØ RunIIb Upgrade

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L1 Calorimeter Trigger

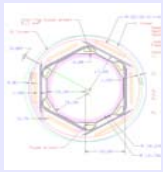
Motivation

- Improve impact parameter resolution.
- Mitigate degradation of silicon performance caused by radiation damage to the SMT inner layers.
- SMT Layer 1 sensors expected to degrade after 3-4 fb^{-1}.
- Important for tracking and b quark tagging at high luminosities.
- Improve B_s mixing measurements

Contributing institutions: Brown, CINVESTAV, Fermilab, Fresno, U. Illinois Chicago, U. Indiana, U. Kansas, Kansas State, Louisiana Tech, U. Mississippi, Michigan State, Moscow State, Northwestern, Rice, Stony Brook, U. Washington, Zurich

Design

- 6-fold symmetry
- 48 silicon sensors
- 96 SVX4 chips
- 12,288 channels



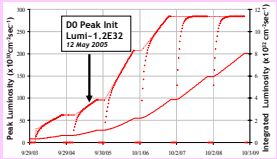
Constraints

Layer Zero must fit between r=16mm (beam pipe) and r=22.8 mm (SMT support structure openings)

Must fit inside existing Run IIa SMT detector

Motivation

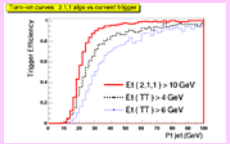
- Accelerator 6-year Plan for Peak & Integrated Luminosities
- L1 trigger limit < 3 KHz. Need more rejection >2.5.



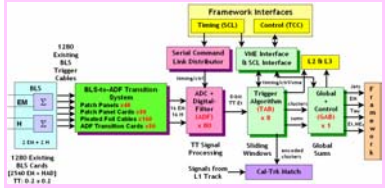
At 2E32 peak lumi & 396 ns bunches

Trigger	Run IIa Definition	Example Channel	L1 Rate [kHz] (no upgrade)	L1 Rate [kHz] (w/ upgrade)
EM	1 EM TT > 10 GeV	W→eν, WH→eνjj	1.3	0.7
DIEM	1 EM TT > 7 GeV 2 EM TT > 5 GeV	Z→ee ZH→eejj	0.5	0.1
e + Jets	1 EM TT > 7 GeV 2 Had TT > 5 GeV	WH→eνjj tt→eν+jets	0.8	0.2
Jet+ME_T	2 TT > 5 GeV ME_T > 10 GeV	ZH→νννbb	2.1	0.8
Calorimeter Rate			4.7	1.8

- Poor E_T resolution for Jet, EM, ME_T trigger objects.
- Slow turn-on curves. 5 GeV trigger tower (TT) thresholds ⇒ 80% efficiency for 40 GeV jets.
- Low thresholds ⇒ unacceptable rates at L = 2E32.



New Electronics



Custom Board	No.	Purpose
ADF: ADC Digital Filter	80	digitize, filter, E-to-E_T.
Serial Command Link Distributor	1	ADF control & timing.
TAB: Trigger Algorithm Board	8	EM & jet sliding window algorithms, Cal-Trk match & L2/L3 outputs, scalar E_T & ME_T sums.
GAB: Global Algorithm Board	1	global E_T & ME_T sums, L2/L3 outputs, AND/OR terms to Trigger Framework.
VME/SCL Board	1	VME control & timing fanout to TAB/GAB.
Patch Panel Cards	80	Converts 16 TT BLS cable** inputs to 2 Pleated Foil Cable (PFC) outputs. TT monitoring.
ATC: ADF Transition Card	80	Converts 2 PFC inputs to ADF Backplane Interface. Sends 3 copies via LVDS cables to TAB.

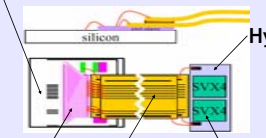
** Constraint - Must reuse cables which carry the trigger pick-off signals from the Calorimeter BLS electronics to the current (and upgrade) electronics.

Contributing institutions: Columbia, Delhi, Dublin, Fermilab, Florida State, U. Illinois Chicago, Michigan State, Northeastern, Rice, Saclay, Southern Methodist, York

Module Components

Silicon Sensor

Radiation hard sensors and chips



Hybrid

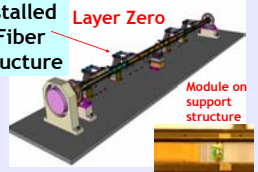
Pitch Adapter

Low mass analog cable

2 SVX4 chips

Modules installed on Carbon Fiber Support Structure

Layer Zero

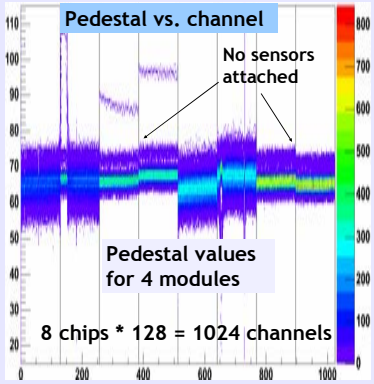


Module on support structure

Hybrid

Module Readout

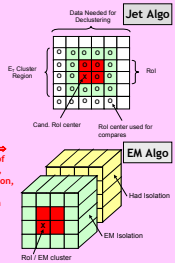
4 Modules installed inside DØ collision hall in November, 2004

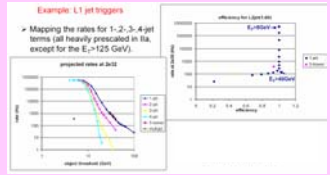


Algorithms

Sliding Windows Algorithm

- E_T cluster local maximum search on 40x32 (ηxφ) TT grid
- Jet, EM & Tau algorithms
- Better calculation of missing E_T
- Topological Triggers
- Jet, EM clustering output for matching with L1 Tracks
- Benefits include 2.5-3x Jet rate reduction assuming constant efficiency. Similar gains for EM &Tau.



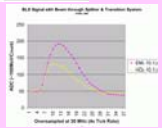


Sidewalk Test Stand

- Stand-alone test stand on "Sidewalk" adjacent to D0 Moveable Counting House
- Tied to Detector ground. Power & safety monitoring.
- Utilize standard D0 DAQ applications.
- Vertical slice - complete signal path from trigger pick-off to test stand electronics to data on tape.

Rack layout for sidewalk test stand. All racks & boards for upgrade will be exercised over >3 mo period before the shutdown.

- Access to real trigger tower data using "Splitter" boards. Designed and built by Saclay. Active split of analog signals at electronics input. 4 TTs per board. Can install up to 4 splitter boards (16 TTs).
- Splitter data - no perturbation of Run IIa L1CAL signals. Allows tests of digital filter algorithm with real data. Can compare TT data from existing and new electronics.



Testing at SiDet

Layer Zero Prototype

- Electrical test stand at SiDet to provide capability for full detector readout.
- Currently reading out 20% of proto-type detector.
- Expected to have full detector readout testing by June.

Layer Zero Installation Structure

SiDet Test Stand

Summary & Schedule

Detector progressing well on all ends.

Running on schedule & within budget!

2005

January - Hybrid Production — Finished!

March - Junction/Adapter Cards — Finished!

April - Module Production — Finished!

June/August - System Tests & Module Installation at SiDet — IN PROGRESS

September - Layer Zero ready to go to DØ

October 3rd - Start of scheduled 3 month Tevatron shutdown

Shutdown - Layer Zero Installation

2005 Highlights

2005

February	Successful ADF-2 review. Complete bench testing of production TABs & GAB. Trigger simulation workshop. Begin design of ADF Transition Card (ATC).
March	Sidewalk test stand ready with racks, power & safety. Build vertical slice starting with ADF & TAB communication/readout. ATC review. Real BLS signals through ADF-2 card.
April	Successful tests between ADF/TAB, TAB/L2, TAB/L3. All 100 production ADF-2 cards completed &tested. Run IIb integrated with TrigSim.
May	Production of pleated foil cables & patch panel cards. ATC prototypes. Successful test of complete L1CAL Run IIb signal path. Data to tape for unpacker development.
June July	Production of 100 ATCs. Full ADF-TAB/GAB testing. Strawman trigger list for Run IIb. Director's review. Add additional splitter cards for real trigger signals during beam. Integrate L1Cal Track match. Label cables.
August September	24/7 running of ADF->TAB/GAB->L2/L3 chain. Unpacker ready. Comparing readout of old and new trigger towers from special runs. Exercise new algorithms with test data.

Shutdown Schedule

Task	Begin	Finish
Tevatron Shutdown for Installation	10/03/05	
Decable BLS cables from existing trigger crates- only component reused for Run IIb	10/05/05	10/12/05
Strip existing trigger racks of old electronics, power supplies, obsolete cables, water lines, etc.	10/13/05	10/21/05
Install new rack infrastructure - power, cooling and safety	10/24/05	10/28/05
Install patch panels, patch panel cards. Relable, redress & reconnect BLS cables.	10/22/05	10/31/05
Install all new crates: ADF, TAB/GAB, Communications. Install new L1CAL trigger control computer. Route & connect additional cables: pleated foil, LVDS, optical, SCL, ECL.	10/31/05	11/14/05
Power up full system. Diagnostic tests. Cable mapping & integrity checks.	11/15/05	11/21/05
Global trigger & detector integration. Calibration. 24/7 running with electronics pulser, cosmics and zero bias. Firmware, control software, trigger terms and algorithm fine tuning.	11/22/05	End of Shutdown